



PTO/SB/08a 07-05

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Substitute for form 1449A/PTO				<i>Complete if Known</i>	
<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(use as many sheets as necessary)</i>				Application Number	10/757 939
				Filing Date	January 16, 2004
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	1	of	10	Attorney Docket Number	43876-153

U. S. PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number-Kind Code <sup>2</sup> (if known)			
11	AA	US-4,852,098	07/25/1989	Brechard, et al.	
	AB	US-4,875,161	10/17/1989	Lahti, et al.	
	AC	US-4,949,294	08/14/1990	Wambergue, et al.	
	AD	US-4,953,073	08/28/1990	Moussouris, et al.	
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	AS	US-5,600,814	02/04/1997	Gahan, et al.	

FOREIGN PATENT DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Foreign Patent Document	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Country Code <sup>3</sup> Number <sup>4</sup> Kind Code <sup>5</sup> (if known)			
11	AT	WO 93/11500			

Examiner Signature	<i>[Signature]</i>	Date Considered	4/10/06
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Sheet	2	of	10	Attorney Docket Number	43876-153

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS					
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.			
<i>HJ</i>	AU	IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications and Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (Mar. 1992) (50006DOC018530 – 563)			
	AV	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)," IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995) (50006DOC018413 – 529)			
	AW	Gerry Kane et al., "MIPS RISC Architecture," Prentice Hall (1995) (50006DOC018576 – 848)			
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	AY	Hewlett-Packard Co., "PA-RISC 1.1 Architecture and Instruction Set," Manual Part No. 09740-90039, (1990) (50006DOC018849 – 19228)			
	AZ	MIPS Computer Systems, Inc., "MIPS R4000 User's Manual," Mfg. Part No. M8-00040, (1990) (50006DOC017026 – 621)			
	BA	i860 <sup>TM</sup> Microprocessor Architecture, Neal Margulis, Foreword by Les Kohn			
	BB	Gove, "The MVP: A Highly-Integrated Video Compression Chip," IEEE Data Compression Conference, pp. 215-24 (March 1994) (51056DOC000891 – 900)			
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	BK	Gwennap, "Digital MIPS Add Multimedia Extensions," Microdesign Resources, pp. 24-28 (November 18, 1996) (51056DOC003454 – 459)			
	BL	Kurpanek et al., "PAT7200: A PA-RISC Processor with Integrated High Performance MP Bus Interface," IEEE COMPCON '94, pp. 375-82 (February 28- March 4, 1994) (51056DOC002149 – 156)			
	BM	Lee et al., "Pathlength Reduction Features in the PA-RISC Architecture," IEEE COMPCON, pp. 129-35 (February 24-28, 1992) (51056DOC068161 – 167)			
BN	Lee et al., "Real-Time Software MPEG Video Decoder on Multimedia-Enhanced PA 7100LC Processors," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 60-68 (April 1995) (51056DOC013549 – 557)				

Examiner Signature	<i>Key 2</i>	Dated Considered	4/10/06
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				Group Art Unit	2183
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## U.S. PATENT DOCUMENTS

## FOREIGN PATENT DOCUMENTS

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INFORMATION DISCLOSURE  
STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet

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of

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## OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS

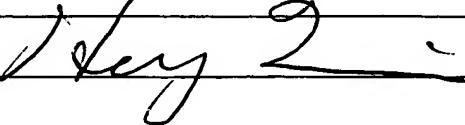
Examiner Initials <sup>1</sup>	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate) title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T <sup>2</sup>
JD	BX	Lee, "Realtime MPEG Video via Software Decompression on a PA-RISC Processor," IEEE, pp. 186-92 (1995) (51056DOC007345 – 351)	
	BY	Martin, "An Integrated Graphics Accelerator for a Low-Cost Multimedia Workstation," Hewlett-Packard Journal, Vol. 46, No. 2, pp. 43-50 (April 1995) (51056DOC072083 – 090)	
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	CA	HP 9000 Series 700 Workstations Technical Reference Manual: Model 712, Hewlett-Packard (January 1994) (51056DOC068048 – 141)	
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	CC	Ang, "StarT Next Generation: Integrating Global Caches and Dataflow Architecture," Proceedings of the ISCA 1992 Dataflow Workshop (1992) (51056DOC071743 – 776)	
	CD	Beckerle, "Overview of the StarT (™) Multithreaded Computer," IEEE COMPCON '93, pp. 148-56 (February 22-26, 1993) (51056DOC002511 – 519)	
	CE	Diefendorff et al., "The Motorola 88110 Superscalar RISC Microprocessor," IEEE pp. 157-62 (1992) (51056DOC008746 – 751)	
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	CG	Nikhil et al., "T: A Multithreaded Massively Parallel Architecture," Computation Structures Group Memo 325-2, Laboratory for Computer Science, Massachusetts Institute of Technology (March 5, 1992) (51056DOC002464 – 476)	
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	CI	Patterson, "Motorola Announces First High Performance Single Board Computer Using Superscalar Chip," Motorola Computer Group (Sept. 1992) (51056DOC069260 – 262)	
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	CK	M. Smotherman et al., "Instruction Scheduling for the Motorola 88110," IEEE, 1993 (51056DOC008784 – 789)	
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	CP	Abel et al., "Extensions to FORTRAN for Array Processing," ILLIAC IV Document No. 235, Department of Computer Science, University of Illinois at Urbana-Champaign (September 1, 1970) (51056DOC001630 – 646)	
	CQ	Barnes et al., "The ILLIAC IV Computer," IEEE Transactions on Computers, Vol. C-17, No. 8, pp. 746-57 (August 1968) (51056DOC012650 – 661)	
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	CS	Awaga et al., "The µVP 64-bit Vector Coprocessor: A New Implementation of High-Performance Numerical Computation," IEEE Micro, Vol. 13, No. 5, pp. 24-36 (October 1993) (51056DOC011921 – 934)	
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Examiner Signature	<i>Devy S</i>	Dated Considered	4/10/06
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	CU	Uchiyama et al., "The Gmicro/500 Superscalar Microprocessor with Branch Buffers," IEEE Micro (October 1993) (51056DOC000185 - 194)			
	CV	Broughton et al., "The S-1 Project: Top-End Computer Systems for National Security Applications," (October 24, 1985) (51056DOC057368 - 607)			
	CW	Farmwald et al., "Signal Processing Aspects of the S-1 Multiprocessor Project," SPIE Vol. 241, Real-Time Signal Processing (1980) (51056DOC072280 - 291)			
	CX	Farmwald, "High Bandwidth Evaluation of Elementary Functions," IEEE Proceedings, 5th Symposium on Computer Arithmetic (1981) (51056DOC071029 - 034)			
	CY	Gilbert, "An Investigation of the Partitioning of Algorithms Across an MIMD Computing System," (February 1980) (51056DOC072244 - 279)			
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	DA	Cornell, S-1 Uniprocessor Architecture SMA-4 (51056DOC056505 - 895)			
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	DC	S-1 Architecture and Assembler SMA-4 Manual, December 19, 1979 (Preliminary Version) (51056DOC057608 - 918)			
	DD	Michielse, "Performing the Convex Exemplar Series SPP System," Proceedings of Parallel Scientific Computing, First Intl Workshop, PARA '94, pp. 375-82 (June 20-23, 1994) (51056DOC020754 - 758)			
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	DF	C4 Technical Overview (September 23, 1993) (51056DOC017111 - 157)			
	DG	Saturn Assembly Level Performance Tuning Guide (January 1, 1994) (51056DOC017369 - 376)			
	DH	Saturn Differences from C Series (February 6, 1994) (51056DOC017150 - 157)			
	DI	"Convex Adds GaAs System," Electronic News (June 20, 1994) (51056DOC019388 - 390)			
	DJ	Convex Architecture Reference Manual, Sixth Edition (1992) (51056DOC016599 - 993)			
	DK	Convex Assembly Language Reference Manual, First Edition (December 1991) (51056DOC015996 - 6598)			
	DL	Convex Data Sheet C4/XA Systems, Convex Computer Corporation (51056DOC059235 - 236)			
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	DN	Convex Notebook containing various "Machine Descriptions" (51056DOC016994 - 7510)			
	DO	"Convex C4/XA Offer 1 GFLOPS from GaAs Uniprocessor," Computergram International, June 15, 1994 (51056DOC019383)			
	DP	Excerpt from Convex C4600 Assembly Language Manual, 1995 (51056DOC061441 - 443)			
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HD	DT	Tyler et al., "AltiVec™: Bringing Vector Technology to the PowerPC™ Processor Family," IEEE (February 1999) (51056DOC071035 - 042)	
	DU	AltiVec™ Technology Programming Environments Manual (1998) (51056DOC071043 - 392)	
	DV	Atkins, "Performance and the i860 Microprocessor," IEEE Micro, pp. 24-27, 72-78 (October 1991) (5156DOC070655 - 666)	
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	ED	Mittal et al., "MMX Technology Architecture Overview," Intel Technology Journal Q3 '97, pp. 1-12 (1997) (5156DOC070689 - 700)	
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	EF	Rhodehamel, "The Bus Interface and Paging Units of the i860 Microprocessor," IEEE, pp. 380-84 (1989) (5156DOC070643 - 647)	
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	EH	Sit et al., "An 80 MFLOPS Floating-Point Engine in the Intel i860 Processor," IEEE, pp. 374-79 (1989) (51056DOC072095 - 101)	
	EI	i860 XP Microprocessor Data Book, Intel Corporation (May 1991) (51056DOC067266 - 427)	
	EJ	Paragon User's Guide, Intel Corporation (October 1993) (51056DOC068802 - 9097)	
	EK	N15 Micro Architecture Specification, dated April 29, 1991 (50781DOC000001 - 982)	
	EL	N15 External Architecture Specification, dated October 17, 1990 (51056DOC017511 - 551)	
	EM	N15 External Architecture Specification, dated December 14, 1990 (50781DOC001442 - 509)	
	EN	N15 Product Requirements Document, dated December 21, 1990 (50781DOC001420 - 441)	
	EO	N15 Product Implementation Plan, dated December 21, 1990 (50781DOC001794 - 851)	
	EP	N12 Performance Analysis document version 2.0, dated September 21, 1990 (51056DOC072992 - 73027)	
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	ER	Mousouris et al., "Architecture of a Broadband MediaProcessor," Microprocessor Forum (1995) (MU0048611 - 630)	

Examiner Signature		Dated Considered	4/10/06
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<p>Substitute for form 1449B/PTO</p> <p><b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b></p> <p><i>(use as many sheets as necessary)</i></p>				<b>Complete if Known</b>	
				Application Number	10/757,939
				Filing Date	January 16, 2004
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	7	of	10	Attorney Docket Number	43876-153

<b>OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS</b>			
Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, page(s), volume-issued number(s), publisher, city and/or country where published.	T <sup>2</sup>
	ES	Arnould et al., "The Design of Nectar: A Network Backplane for Heterogeneous Multicomputers," ACM (1989) (51056DOC020947 - 958)	
	ET	Bell, "Ultracomputers: A Teraflop Before Its Time," Communications of the ACM, (August 1992) pp. 27-47 (51056DOC020903 - 923)	
	EU	Broomell et al., "Classification Categories and Historical Development of Circuit Switching Topologies," Computing Surveys, Vol. 15, No. 2, pp 95-133 (June 1983) (51056DOC003002 - 040)	
	EV	Culler et al., "Analysis of Multithreaded Microprocessors Under Multiprogramming," Report No. UCB/CSD 92/687 (May 1992) (51056DOC069283 - 300)	
	EW	Donovan et al., "Pixel Processing in a Memory Controller," IEEE Computer Graphics and Applications, pp. 51-61 (January 1995) (51056DOC059635 - 645)	
	EX	Fields, "Hunting for Wasted Computing Power: New Software for Computing Networks Puts Idle PC's to Work," Univ. of Wisconsin-Madison, <a href="http://www.cs.wisc.edu/condor/doc/Wiscldea.html">http://www.cs.wisc.edu/condor/doc/Wiscldea.html</a> (1993) (51056DOC068704 - 711)	
	EY	Geist, "Cluster Computing: The Wave of the Future?," Oak Ridge National Laboratory, 84OR21400 (May 30, 1994) (51056DOC020924 - 929)	
	EZ	Ghafoor, "Systolic Architecture for Finite Field Exponentiation," IEEE Proceedings, Vol. 136 (November 1989) (51056DOC071700 - 705)	
	FA	Gilioi, "Parallel Programming Models and their Interdependence with Parallel Architectures," IEEE Proceedings (September 1993) (51056DOC071792 - 801)	
	FB	Hwang et al., "Parallel Processing for Supercomputers and Artificial Intelligence," (1993) (51056DOC059663 - 673)	
	FC	Hwang, "Advanced Computer Architecture: Parallelism, Scalability, Programmability," (1993) (51056DOC059656 - 662)	
	FD	Hwang, "Computer Architecture and Parallel Processing," McGraw Hill (1984) (51056DOC070166 - 1028)	
	FE	Iwaki, "Architecture of a High Speed Reed-Solomon Decoder," IEEE Consumer Electronics (January 1994) (51056DOC071687 - 694)	
	FF	Jain et al., "Square-Root, Reciprocal, SINE/COSINE, ARCTANGENT Cell for Signal and Image Processing," IEEE ICASSP '94, pp. II-521 - II-524 (April 1994) (51056DOC003070 - 073)	
	FG	Laudon et al., "Architectural and Implementation Tradeoffs in the Design of Multiple-Context Processors," Technical Report: CSL-TR-92-523 (May 1992) (51056DOC069301 - 327)	
	FH	Lawrie, "Access and Alignment of Data in an Array Processor," IEEE Transactions on Computers, Vol. C-24, No. 12, pp. 99-109 (December 1975) (51056DOC002932 - 942)	
	FI	Le-Ngoc, "A Gate-Array-Based Programmable Reed-Solomon Codec: Structure-Implementation-Applications," IEEE Military Communications (1990) (51056DOC071695 - 699)	
	FJ	Litzkow et al., "Condor – A Hunter of Idle Workstations," IEEE (1988) (51056DOC068712 - 719)	
	FK	Markstein, "Computation of Elementary Functions on the IBM RISC System/6000 Processor," IBM J. Res. Develop., Vol. 34, No. 1, pp 111-19 (January 1990) (51056DOC059620 - 628)	
	FL	Nienhaus, "A Fast Square Rooter Combining Algorithmic and Table Lookup Techniques," IEEE Proceedings Southeastcon, pp. 1103-05 (1989) (51056DOC061469 - 471)	
FM	Renwick, "Building a Practical HIPPI LAN," IEEE, pp. 355-60 (1992) (51056DOC020937 - 942)		

Examiner Signature		Dated Considered	4/14/06
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<i>(use as many sheets as necessary)</i>				Filing Date	January 16, 2004
				First Named Inventor	Craig C. HANSEN, et al.
				Group Art Unit	2183
				Examiner Name	CHAN, EDDIE P
Sheet	8	of	10	Attorney Docket Number	43876-153

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS					
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CH	FN	Rohrbacher et al., "Image Processing with the Staran Parallel Computer," IEEE Computer, Vol. 10, No. 8, pp. 54-59 (August 1977) (reprinted version pp. 119-124) (51056DOC002943 - 948)			
	FO	Ryne, "Advanced Computers and Simulation," IEEE, pp. 3229-33 (1993) (51056DOC020883 - 887)			
	FP	Siegel, "Interconnection Networks for SIMD Machines," IEEE Computer, Vol. 12, No. 6 (June 1979) (reprinted version pp. 110 118) (51056DOC002949 - 957)			
	FQ	Singh et al., "A Programmable HIPPI Interface for a Graphics Supercomputer," ACM (1993) (51056DOC020888 - 896)			
	FR	Smith, "Cache Memories," Computing Surveys, Vol. 14, No. 3 (September 1982) (51056DOC071586 - 643)			
	FS	Tenbrink et al., "HIPPI: The First Standard for High-Performance Networking," Los Alamos Science (1994) (51056DOC020943 - 946)			
	FT	Tolmie, "Gigabit LAN Issues: HIPPI, Fibre Channel, or ATM," Los Alamos National Laboratory Report No. LA-UR 94-3994 (1994) (51056DOC046599 - 609)			
	FU	Tolmie, "HIPPI: It's Not Just for Supercomputers Anymore," Data Communications (May 8, 1995) (51056DOC071802 - 809)			
	FV	Toyokura et al., "A Video DSP with a Macroblock-Level-Pipeline and a SIMD Type Vector-Pipelined Architecture for MPEG2 CODEC," ISSCC94, Section 4, Video and Communications Signal Processors, Paper WP 4.5, pp. 74-75 (1994) (51056DOC003659 - 660)			
	FW	Tullsen et al., "Simultaneous Multithreading: Maximizing On-Chip Parallelism," Proceedings of the 22nd Annual International Symposium on Computer Architecture (June 1995) (51056DOC071434 - 443)			
	FX	Turcotte, "A Survey of Software Environments for Exploiting Networked Computing Resources," Engineering Research Center for Computational Field Simulation (June 11, 1993) (51056DOC069098 - 256)			
	FY	Vetter et al., "Network Supercomputing: Connecting Cray Supercomputers with a HIPPI Network Provides Impressively High Execution Rates," IEEE Network (May 1992) (51056DOC020930 - 936)			
	FZ	Wang, "Bit-Level Systolic Array for Fast Exponentiation in GF(2 <sup>m</sup> )," IEEE Transactions on Computers, Vol. 43, No. 7, pp. 838-41 (July 1994) (51056DOC059407 - 410)			
	GA	Ware et al., "64 Bit Monolithic Floating Point Processors," IEEE Journal of Solid-State Circuits, Vol. Sc-17, No. 5 (October 1982) (51056DOC059646 - 655)			
	GB	"Bit Manipulator," IBM Technical Disclosure Bulletin, pp. 1575-76 (November 1974) (51056DOC010205 - 206)			
	GC	Finney et al., "Using a Common Barrel Shifter for Operand Normalization, Operand Alignment and Operand Unpack and Pack in Floating Point," IBM Technical Disclosure Bulletin, pp. 699-701 (July 1986) (51056DOC010207 - 209)			
	GD	Data General AViiON AV500, 550, 4500 and 5500 Servers			
	GE	Jovanovic et al., "Computational Science: Advances Through Collaboration," San Diego Supercomputer Center Science Report (1993) (51056DOC068769 - 779)			
	GF	High Performance Computing and Communications: Toward a National Information Infrastructure, National Science Foundation (NSF) (1994) (51056DOC068791 - 801)			
	GG	National Coordination Office for High Performance Computing and Communications, "High Performance Computing and Communications: Foundation for America's Information Future" (1996) (51056DOC072102 - 243)			
CH	GH	Wilson, "The History of the Development of Parallel Computing," <a href="http://ei.cs.vt.edu/~history/Parallel.html">http://ei.cs.vt.edu/~history/Parallel.html</a> (51056DOC068720 - 757)			

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				Filing Date	January 16, 2004
				First Named Inventor	Craig C. HANSEN, et al.
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Sheet	9	of	10	Attorney Docket Number	43876-153

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<i>HD</i>	GI	IEEE Standard 754 (ANSI/IEEE Std. 754-1985) (51056DOC019304 - 323)			
		Original Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed March 26, 2004			
	GJ	Amended Complaint for Patent Infringement, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed April 20, 2004			
	GK	Expert Witness Report of Richard A. Killworth, Esq., <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005			
	GL	Declaration and Expert Witness Report of Ray Mercer Regarding Written Description and Enablement Issues, <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 12, 2005			
	GM	Corrected Expert Report of Dr. Stephen B. Wicker Regarding Invalidity of U.S. Patent Nos. 5,742,840; 5,794,060; 5,764,061; 5,809,321; 6,584,482; 6,643,765; 6,725,356 and Exhibits A-I; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 6, 2005			
	GN	Defendants Intel and Dell's Invalidity Contentions with Exhibits A-G; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed September 19, 2005			
	GO	Defendants Dell Inc. and Intel Corporation's Identification of Prior Art Pursuant to 35 USC §282; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division filed October 7, 2005			
	GP	Request for <i>Inter Partes</i> Reexamination Under 35 USC §§ 311-318 of U.S. Patent No. 6,725,356 filed on June 28, 2005			
	GQ	Deposition of Larry Mennemeier on September 22, 2005 and Exhibit 501; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division			
	GR	Deposition of Leslie Kohn on September 22, 2005; <i>MicroUnity Systems Engineering, Inc. v. Dell, Inc. /k/a/ Dell Computer and Intel Corporation</i> ; C.A. NO. 2-04CV-120; In the United States District Court of the Eastern District of Texas, Marshall Division			
	GS	Intel Article, "Intel Announces Record Revenue of 9.96 Billion", October 18, 2005			
	GT	The New York Times Article, "Intel Posts 5% Profit Increase on Demand for Notebook Chips", October 19, 2005			
	GU	USA Today Article, "Intel's Revenue Grew 18% In Robust Quarter for Tech", October 19, 2005			
	GV	The Wall Street Journal Article, "Intel Says Chip Demand May Slow", October 19, 2005			
<i>HD</i>	GW	The New York Times Article, "Intel Settlement Revives A Fading Chip Designer", October 20, 2005			

Examiner Signature	<i>Hay S</i>	Dated Considered	4/10/06
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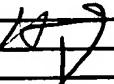
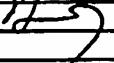
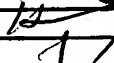
INFORMATION DISCLOSURE CITATION IN AN APPLICATION				ATTY. DOCKET NO. <b>043876-0153</b>	SERIAL NO. <b>10/757,939</b>	
				APPLICANT <b>Craig HANSEN, et al.</b>		
(PTO-1449)				FILING DATE <b>January 16, 2004</b>	GROUP <b>2183</b>	
				U.S. PATENT DOCUMENTS		
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code <sub>2</sub> ( <i>if known</i> )	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document		Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
<i>MH3</i>	A	US 6,643,765	11-04-2003	Hansen et al.		
	B	US 6,725,356	04-20-2004	Hansen et al.		
	US					
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FOREIGN PATENT DOCUMENTS						
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code <sub>2</sub> - Number « - Kind Codes ( <i>if known</i> )	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes      No
OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)						
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.				
<i>MH3</i>	C	MARKOFF, JOHN, "Intel Settlement Revives a Fading Chip Designer," The New York Times (10-20-2005)				
	D	Intel Press Release, "Intel Announces Record Revenue of \$9.96 Billion," Santa Clara, CA, 10-18-2005				
<i>MH3</i> EXAMINER			DATE CONSIDERED <i>4/10/06</i>			

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JUN 10 2005  
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SHEET 1 OF 11

INFORMATION DISCLOSURE CITATION IN AN APPLICATION  (PTO-1449)				ATTY. DOCKET NO. <b>043876-0153</b>	SERIAL NO. <b>10/757,939</b>			
				APPLICANT <b>HANSEN, C., et al.</b>				
				FILING DATE <b>January 16, 2004</b>	GROUP <b>2183</b>			
<b>U.S. PATENT DOCUMENTS</b>								
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code(s if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear			
	US	4,658,349 A	05/14/1987	Gafken				
	US	4,852,098	07/25/1989	Brechard et al.				
	US	4,875,161	10/17/1989	Lahti				
	US	4,948,294	08/14/1990	Wambergue				
	US	4,953,073	08/28/1990	Moussouris et al.				
	US	4,959,779	09/25/1990	Weber et al.				
	US	5,113,508	05/12/1992	Moussouris et al.				
	US	5,161,247	11/3/1992	Murakami et al.				
	US	5,208,914	05/04/1993	Wilson et al.				
	US	5,231,648	07/27/1993	Health et al				
	US	5,233,690	08/03/1993	Shelock et al.				
	US	5,268,895	12/07/1993	Diefendorff et al.				
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	US	5,430,660 A	07/04/1995	John Hengeveld et al.				
	US	5,471,628	11/28/1995	Phillips et al.				
	US	5,515,520	05/07/1996	Hatta et al.				
	US	5,533,185	07/02/1996	Lentz et al.				
	US	5,590,385	12/31/1996	Ide et al.				
	US	5,638,351	06/03/1997	Lee				
	US	5,742,840	04/21/1998	Hansen et al.				
	US	5,778,412 A	07/07/1998	Gafken				
	US	5,828,869	10/27/1998	Johnson et al.				
	US	5,996,057	11/30/1999	Scales, III et al.				
		US	6,453,368 B2	09/17/2002	Yamamoto			
		US	6,857,908 B1	05/20/2003	Furuhashi			
	<b>FOREIGN PATENT DOCUMENTS</b>							
	EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Code(s)-Number & Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
			JP 3268024	11/28/1991	Hitachi Ltd.			
			EP 0 468 820 A2	01/29/1992	Fujitsu Limited			
		WO 93/01565	01/21/1993	Seiko Epson Corporation				
		CA 1 323 451	10/19/1993	Northern Telecom Ltd.				
		JP 6095843	04/08/1994	IBM				
		EP 0 651 321 A	05/03/1995	Advanced Micro Devices Inc.				
		EP 0 654 733 A1	05/24/1995	Hewlett-Packard				
		JP-S80-217435	10/31/1985	Toshiba Corp.				
		WO 97/07450	02/27/1997	Microunity Systems Engineering, Inc.				
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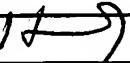
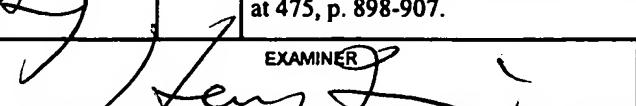
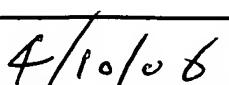
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	L-114	McKee, et. al., "Bounds on Memory Bandwidth in Streamed Computations," Computer Science Report CS-95-32, March 1, 1995.	
EXAMINER		DATE CONSIDERED	

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<b>INFORMATION DISCLOSURE CITATION IN AN APPLICATION</b>  <b>(PTO-1449)</b>		ATTY. DOCKET NO. <b>043876-0153</b>	SERIAL NO. <b>10/757,939</b>
<b>APPLICANT</b> <b>HANSEN, C., et al.</b>			
		FILING DATE <b>January 16, 2004</b>	GROUP <b>2183</b>
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>			
EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	
<i>HJ</i>	L-115	McKee, Sally A., "Maximizing Memory Bandwidth for Streamed Computations," A Dissertation Presented to the Faculty of the School of Engineering and Applied Science at the University of Virginia, May 1995.	
	L-116	A Systematic Approach to Optimizing and Verifying Synthesized High-Speed ASICs", Trevor Landon, et. Al. , Computer Science Report No. CS-95-51, December 11, 1995.	
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	L-124	Baland, Granito, Marcotte, Messina, Smith, "The IBM System1360 Model 91 : Storage System" IBM System Journal, January, 1967, pp. 54-68.	
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	L-127	S.S. Reddi et. al. "A Conceptual Framework for Computer Architecture" Computing Surveys., Vol. 8, No. 2, June 1976.	
<i>HJ</i>	L-128	Yulun Wang, et al, "The 3DP: A processor Architecture for Three-Dimensional Applications, January 1992, p. 25-36.	
EXAMINER <i>Henry J.</i>	DATE CONSIDERED <i>4/10/08</i>		

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		FILING DATE <b>January 16, 2004</b>	GROUP <b>2183</b>
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>			
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<i>HS</i>	L-129	"IEEE Draft Standard for High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", 1995, pp.1-104, IEEE.	
<i>1</i>	L-130	Gerry Kane and Joe Heinrich, "MIPS RISC Architecture" 1992, Publisher: Prentice-Hall Inc., A Simon & Shuster Company, Upper Saddle River New Jersey.	
	L-131	CATHY MAY et al. "The Power PC Architecture: A Specification For A New Family of Risc Processors" Second Edition May 1994, pp. 1—518, Morgan Kaufmann Publishers, Inc. San Francisco CA, IBM International Business Machines, Inc.	
	L-132	"IEEE Standard for Scalable Coherent Interface (SCI)", Published by the Institute of Electrical and Electronics Engineers, Inc. August 2, 2003, pp. 1-248.	
	L-133	DON TOLMIE and Don Flanagan, "HIPPI: It's Not Just for Supercomputers Anymore" Data Communications published May 8, 1995.	
	L-136	IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X May 1995.	
	L-137	JOE HEINRICH, "MIPS R4000 Microprocessor User's Manual Second Edition" 1994 MIPS Technologies, Inc. pp. 1-754.	
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	L-139	Ang, StarT Next Generation: Integrating Global Caches and Dataflow Architecture, Proceedings of the ISCA 1992.	
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	L-142	Convex 3400 Supercomputer System Overview, published July 24, 1991.	
	L-143	Gilio, Parallel Programming Models and Their Interdependence with Parallel Architectures, IEEE Proceedings published September 1993.	
	L-144	PCT International Search Report and Written Opinion dated March 11, 2005, corresponding to PCT/US04/22126	
<i>HS</i>	L-145	Supplementary European Search Report dated March 18, 2005, corresponding to Application No. 96928129.4	
EXAMINER <i>Dee</i>		DATE CONSIDERED <i>4/14/08</i>	

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SHEET 1 OF 3

INFORMATION DISCLOSURE CITATION IN AN APPLICATION  (PTO-1449)		ATTY. DOCKET NO. <b>43876-153</b>	SERIAL NO. <b>Continuation of Serial No. 10/646,787</b>				
APPLICANT <b>HANSEN, et al.</b>							
		FILING DATE <b>January 16, 2004</b>	GROUP <b>To be assigned</b>				
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
1H	4,025,772	05/24/77	Constant				
	4,489,393	12/18/84	Kawahara, et al.				
	4,701,875	10/20/87	Konishi, et al.				
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	4,876,660	10/24/89	Owens, et al.				
	4,893,267	01/09/90	Alsup, et al.				
	4,956,801	09/11/90	Priem et al.				
	4,969,118	11/06/90	Montoye, et al.				
	4,975,868	12/04/90	Freerksen				
	5,032,865	07/16/91	Schlunt				
	5,157,388	10/20/92	Kohn				
	5,201,056	04/06/93	Daniel, et al.				
	5,268,855	12/07/93	Mason, et al.				
2H	5,268,995	12/07/93	Diefendorff, et al.				
<b>FOREIGN PATENT DOCUMENTS</b>						Translation	
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Yes	No
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
1H	Parallel Computers for Graphics Applications, Adam Levinthal, Pat Hanrahan, Mike Paquette, Jim Lawson, Pixar San Rafael, California, 1987						
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2H	Microprocessor Report, Volume 7 Number 13, October 4, 1993, IBM Regains Performance Lead with Power2, Six Way Superscalar CPU in MCM Achieves 126 SPECint92.						
	IBM Creates PowerPC Processors for AS/400, Two New CPU's Implement 64-Bit Power PC with Extensions by Linley Gwennap, July 31, 1995.						
EXAMINER <i>Henry Jan</i>	DATE CONSIDERED 4/10/06						

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APPLICANT <b>HANSEN, et al.</b>						
FILING DATE <b>January 16, 2004</b>		GROUP <b>To be assigned</b>				
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE
<i>AS</i>	5,408,581	04/18/95	Suzuki, et al.			
<i>AS</i>	5,423,051	06/06/95	Fuller, et al.			
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<i>AS</i>	5,500,811	03/19/96	Corry			
<i>AS</i>	5,557,724	09/17/96	Sampat, et al.			
<i>AS</i>	5,588,152	12/24/96	Dapp, et al.			
<i>AS</i>	5,592,405	01/07/97	Gove, et al.			
<i>AS</i>	5,640,543	06/17/97	Farrell, et al.			
<i>AS</i>	5,642,306	06/24/97	Mennemeier, et al.			
<i>AS</i>	5,666,298	09/09/97	Peleg, et al.			
<i>AS</i>	5,669,010	09/16/97	Duluk, Jr.			
<i>AS</i>	5,673,407	09/30/97	Poland, et al.			
<i>AS</i>	5,675,526	10/07/97	Peleg, et al.			
<i>AS</i>	5,680,338	10/21/97	Agarwal, et al.			
<b>FOREIGN PATENT DOCUMENTS</b>						
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Translation
						Yes
<i>AS</i>	0 474 246 A2	06/09/91	Europe			
<i>AS</i>	0 654 733 A1	05/07/94	Europe			
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>						
<i>AS</i>	The Visual Instruction Set (VIS) in UltraSPAR <sup>TM</sup> , L. Kohn, G. Maturana, M. Tremblay, A. Prabhu, G. Zyner, May 3, 1995, 462-469					
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EXAMINER	<i>Larry J.</i>		DATE CONSIDERED		4/10/06	

INFORMATION DISCLOSURE CITATION IN AN APPLICATION			ATTY. DOCKET NO. <b>43876-153</b>	SERIAL NO. <b>Continuation of Serial No. 10/646,787</b>			
			APPLICANT <b>HANSEN, et al.</b>				
(PTO-1449)			FILING DATE <b>January 16, 2004</b>	GROUP <b>To be assigned</b>			
<b>U.S. PATENT DOCUMENTS</b>							
EXAMINER'S INITIALS	PATENT NO.	DATE	NAME	CLASS	SUBCLASS	FILING DATE	
<i>HS</i>	5,721,892	02/24/98	Peleg, et al.				
<i>✓</i>	5,734,874	03/31/98	Van Hook, et al.				
	5,757,432	05/26/98	Dulong, et al.				
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	6,092,094	07/18/00	Ireton				
<i>✓</i>	6,401,194 B1	06/04/02	Nguyen, et al.				
<b>FOREIGN PATENT DOCUMENTS</b>						Translation	
EXAMINER'S INITIALS	PATENT NO.	DATE	COUNTRY	CLASS	SUBCLASS	Yes	No
<b>OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)</b>							
EXAMINER <i>Neenay</i>	DATE CONSIDERED <i>4/10/06</i>						

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SHEET 1 OF 1

INFORMATION DISCLOSURE CITATION IN AN APPLICATION  (PTO-1449)				ATTY. DOCKET NO. 43876-153	SERIAL NO. Continuation of Serial No. 10/646,787	
				APPLICANT Craig HANSEN, et al.		
				FILING DATE January 16, 2004	GROUP To be assigned	
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code <sub>2</sub> ( <i>if known</i> )	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
<i>HS</i>	US	4,785,393	11/15/1988	Chu et al.		
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	US	5,031,135	07/09/1991	Patel		
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	US	5,600,814	02/1997	Gahan et al.		
	US	5,740,093	04/14/1998	Sharangpani		
	US	5,742,840	04/21/1998	Hansen et al.		
	US	5,768,546	06/1998	Kwon		
	US	5,898,849	04/27/1999	Tran		
	US	5,996,057	11/30/1999	Hunter L. Scales, III, et al.		
	US	6,041,404	03/21/2000	Patrice Roussel, et al.		
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<b>FOREIGN PATENT DOCUMENTS</b>						
EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number +-Kind Codes ( <i>if known</i> )	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation
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<i>HS</i>		IEEE Draft Standard for "Scalable Coherent Interface-Low-Voltage Differential Signal Specifications And Packet Encoding", IEEE Standards Department, P1596.3/D0.15 (March 1992)				
		IEEE Draft Standard for "High-Bandwidth Memory Interface Based on SCI Signaling Technology (RamLink)", IEEE Standards Department, Draft 1.25 IEEE P1596.4-199X (May 1995)				
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<i>Kerry Tran</i>			DATE CONSIDERED <i>4/10/06</i>			

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SHEET 1 OF 1

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				<b>APPLICANT</b> <b>Craig HANSEN et al</b>		
				<b>FILING DATE</b> <b>Jan. 16, 2004</b>	<b>GROUP</b> <b>To be assigned</b>	
<b>U.S. PATENT DOCUMENTS</b>						
EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Code (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	
<i>1/10/06</i>	US	5,819,101	10/6/1998	Alexander Peleg, et al		
<i>1/10/06</i>	US	5,881,275	3/9/1999	Alexander Peleg, et al		
<i>1/10/06</i>	US	6,119,216	9/12/2000	Alexander Peleg, et al		
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<i>1/10/06</i>	US					
<i>1/10/06</i>	US					
<i>1/10/06</i>	US					
<i>1/10/06</i>	US					
<b>FOREIGN PATENT DOCUMENTS</b>						
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